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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,216	08/30/2000	Tongbi Jiang	M4065.0227/P227	2311

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EXAMINER	
PERT, EVAN T	
ART UNIT	PAPER NUMBER
2813	7

DATE MAILED: 12/21/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/652,216	JIANG ET AL.	
	Examiner	Art Unit	
	Evan T. Pert	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-99* is/are pending in the application.

4a) Of the above claim(s) *31-65* is/are withdrawn from consideration.

5)☐ Claim(s) ____ is/are allowed.

6)☒ Claim(s) *1-30 and 66-99* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-30 and 66-99 in Paper No. 4 is acknowledged. Claims 1-30 and 66-99 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected invention, there being no allowable generic or linking claim.

Drawings

2. The drawings are objected to because Fig. 5 is not a cross-section of line V-V in Fig. 4 as implied by the last line of page 4. A proposed drawing correction is required in reply to the Office action.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-7, 9-30, 66-67, 69-72 and 74-96 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in view of the "Intel 2000 Packaging Databook" ("Intel").

AAPA

Applicant admits that semiconductor devices having transistors (well known as "electrical elements") are commonly fabricated in the upper active surface of a semiconductor substrate wherein a plurality of "well plugs" are commonly provided to act as a means for receiving and providing a bias voltage to the well region(s) of the substrate in order to adjust threshold voltage [pages 1-2].

Claim 1

Applicant's claim 1 recites AAPA at lines 1-6 with "a conductive layer provided on a back side of said substrate" at line 7, wherein "substrate" is taken to mean "any semiconductor-based structure that has an exposed silicon surface" [page 5, lines 12-13].

By applicant's definition of "substrate", a bare "chip" or "die" which has been diced from a wafer substrate is also a called a "substrate" which corresponds to the block labeled "Silicon" in Intel's Figures 3-1 through 3-4 on their pages 3-2 to 3-3.

It would have been obvious at the time of applicant's invention to provide a a conductive layer on a back side of the (die) (chip) substrate as is depicted by Intel, motivated by functional benefits in the final packaging such the ability to perform substrate biasing, heat sinking, and /or to "provide a readily wetted surface" [Intel, Section 3.3.1].

Claim 2

AAPA teaches "transistors" which are *inherent* to well known DRAM memory devices, processor devices, and logic devices.

Claim 4

AAPA teaches "conductive plugs" for coupling the bias voltage source to distribution regions [see also, for example, col. 1, lines 46-49 of U.S. Patent 6,048,746].

Claim 5

Intel teaches a "metallic" layer which has the desirable "metallic" quality of being electrically conductive [Section 3.3.3.5].

Claims 6, 14 and 23

Intel teaches that "it is important to control thickness" [Section 3.3.4.3] and one of ordinary skill in the art would be motivated to make the "conductive metallic layer" as thin as possible (i.e. "less than or equal to 10 mil") in order to achieve the lowest possible ohmic resistance *through* the layer.

Likewise, it would have been obvious to provide conductive "paste" at a thickness as close to zero as possible, such that the layer of paste is provided less than 1 mil. One of ordinary skill in the art would be motivated to apply a layer less than 1 mil thick in order to achieve a lower resistance *through* the layer, closer to an ideal "ohmic" resistance of zero ohms.

Claim 7

Intel teaches an embodiment wherein a metallic layer is secured to the substrate back side with "conductive adhesive" [Figure 3-4].

Claims 9, 15, 20 and 24

Intel teaches that an "ohmic contact" may be desired to the back-side of the die wherein "ohmic" is understood by one of ordinary skill in the art to mean a very low resistance. It would have been obvious to chose a conductive layer having a resistivity as close to zero as is possible, merely by design choice. One of ordinary skill in the art would be motivated to chose a material having a resistivity of near zero, to obtain as ideal an ohmic contact to the back side as is possible, as is taught by Intel.

Claims 10 and 11

Intel teaches at least silver, gold and copper (Figure 3-4).

Claim 12

Intel teaches the conductive layer having a length exceeding the length of die-chip-substrate [Fig. 3-1].

Claim 13

Intel teaches a silver-filled "adhesive" and Cyanate Ester, which can be considered to be a "cured conductive paste" after drying.

Claims 16-18 and 21

The adhesive polymer (corresponding to applicant's "paste") taught by Intel is filled with silver (conductive) particles [see Figure 3-4 for example], wherein said adhesive is *inherently* isotropically conductive because Intel does not speak of any anisotropic qualities.

Claim 19

While one of ordinary skill in the art would be motivated to minimize film thickness, one would also need a good bond [Intel, Section 3.3.4.2]. It would be a mere matter of experimentation with the teaching of Intel to determine an appropriate thickness for an adequate bond. One of ordinary skill in the art would be motivated to provide a layer thicker than 1 mil if such was required for a good mechanical bond, merely by design choice (even though a thinner layer is desirable to lower resistance).

Claims 22, 25-26

Intel shows a silver or gold "film" metallization as the "conductive layer" on the backside of the "substrate" [Fig. 3-1].

Claims 27-30

The examiner takes Official Notice that, at the time of applicant's filing, DRAM memory devices, logic devices and processor devices were well known to contain transistors subject to threshold variations from "body effects", wherein all such devices benefit from a backside metal layer in packaging as taught by Intel. For example, U.S. Patent 6,091,140 (packaging "chip" substrates) teaches, "the silicon chip (substrate) 30 can be, for example, an integrated circuit component such as a *DRAM*, a SDRAM, an EPROM, a *LOGIC*, a microprocessor or a digital signal *processor* chip [col. 5, lines 42-45].

Claims 66-67, 69-72 and 74-95

Claims 66-67, 69-72 and 74-95 are the same as claims 1-2, 4-7 and 9-30 as discussed above, except that the "substrate" (a.k.a. "chip") (a.k.a. "die") acts as a "processor" with a memory device in communication with said processor.

The chip packaging techniques taught by Intel are obviously applicable to "processors" since this is what Intel is known for making. That is, it would have been obvious to provide a chip utilizing AAPA well-tie biasing along with packaging in accordance with Intel's Packaging Databook. One of ordinary skill in the art would be motivated to provide the metal layer on the die backside for reasons taught by Intel [Section 3.3.1].

Claim 96

In Fig. 3-1 of Intel, the "substrate" is marked "Silicon", but the alumina body is not a "substrate" by applicant's definition (i.e. "no exposed silicon"), so an electrical path is established from the "substrate" to a "non-substrate" area, in the corner of the alumina recess where metal film reaches, for example.

Claims 3, 8, 68, 73 and 97

5. Claims 3, 8, 68, 73 and 97 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Intel as applied to claims 1, 5, 66 and 70 above, and further in view of Burr (U.S. Patent 5,753,958).

AAPA and Intel are silent with respect to explicitly naming "what" electrical source the metallic backside layer should be connected to and exactly "how" it should be connected.

Yet, Intel does suggest that a backside metallic layer is useful for establishing "backside bias" [Section 3.3.1], motivating one of ordinary skill in the art to connect the metallic layer to a substrate bias source, such as the substrate bias source taught by Burr et al. [abstract]. For example, Burr et al. shows a backside contact "B" with metallic layer "106" on the backside.

It would have been obvious to provide the AAPA with a metallic back-side layer by the packaging considerations of Intel, and it would have been obvious to connect the added backside layer to a substrate bias voltage source to attain a control of substrate backside biasing, as is referenced by Intel, for example, in Section 3.3.1.

Claims 98 and 99

6. Claims 98 and 99 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Intel as applied to claim 1 above and further in view of Worley et al. (U.S. Patent 6,147,857).

In claim 98, lines 1-6 are AAPA [see above].

In claim 99, lines 1-6 are AAPA [see above].

Claims 98 and 99, lines 7+ recite that a backside (metallic) layer is provided such that it is wire-bonded to another area or a bonding pad of the device. Intel speaks of wire bonding, but not directly with respect to a backside layer [Section 3.4].

Worley et al. teach an optional bypass capacitor that has the backside metal layer acting as a capacitor electrode wherein the backside 311 is wire-bonded by bonding wire 310 to pad 309.

It would have been obvious to provide the optional by-pass capacitor in the invention of AAPA, for the benefits of an on-chip by-pass capacitor (reduced noise). In providing the backside layer (electrode), one of ordinary skill in the art would be motivated to chose wire bonding for electrical connection at the suggestion of Worley et al. [Fig. 3 taken with col. 5, lines 14-19].

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Burr et al. (U.S. Patent 5,753,958) is cited for teaching well ties for back biasing to adjust threshold voltage, as in AAPA.

Toh et al. is cited for teaching the well known fact that "chips" needing to be packaged, as in the teachings of Intel, include chips that perform "various functions" wherein said functions include DRAM memories, processors, and "logic" [see the "various functions" at page 1, line 5 of applicant's specification].

The Intel 1998 PACKAGING DATABOOK is cited for teaching the definition of "Backside bias" known to one of ordinary skill in the art: "The electrical connection to the backside of the silicon device used to ensure proper performance" [Page 1 of Glossary].

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers can be reached on 703-308-2417. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ETP
December 11, 2001

EVAN PERT